

Low Jitter Clock Generators for Set-Top Box

The ISL14010 series of devices are general purpose integrated Clock Synthesizers and Generators suited for consumer applications such as Set-top Box, and various other consumer applications.

The selectable reference input accepts 30MHz signal either from crystal or an external source. It is specified to operate with a nominal 3.3V supply and is offered in 16 Ld QFN package.

Contact Factory for other output frequency options.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL14010IRZ*	10IZ	-40 to +85	16 LD QFN	L16.3x3
ISL14017IRZ*	17IZ	-40 to +85	16 LD QFN	L16.3x3

*Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Selection Table

PART OPTIONS	INPUT FREQUENCY	NUMBER OF OUTPUTS	OUTPUT FREQUENCY	PACKAGE
ISL14010	30MHz	4 LVTTL	25, 30, 48, 54	16 LD QFN
ISL14017	30MHz	4 LVTTL	25, 30, 40, 50	16 LD QFN

Features

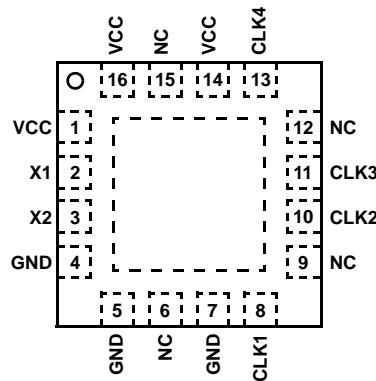
- LVTTL Outputs
- Selectable Crystal or Ref. Clock for Inputs
- Period Jitter ~50ps RMS
- Single Supply; 3.3V nominal
- Extended Temperature Range: -40°C to +85°C
- Available in small foot print package
 - 16 Ld QFN 3mmx3mm
- Pb-Free plus anneal available (RoHS Compliant)

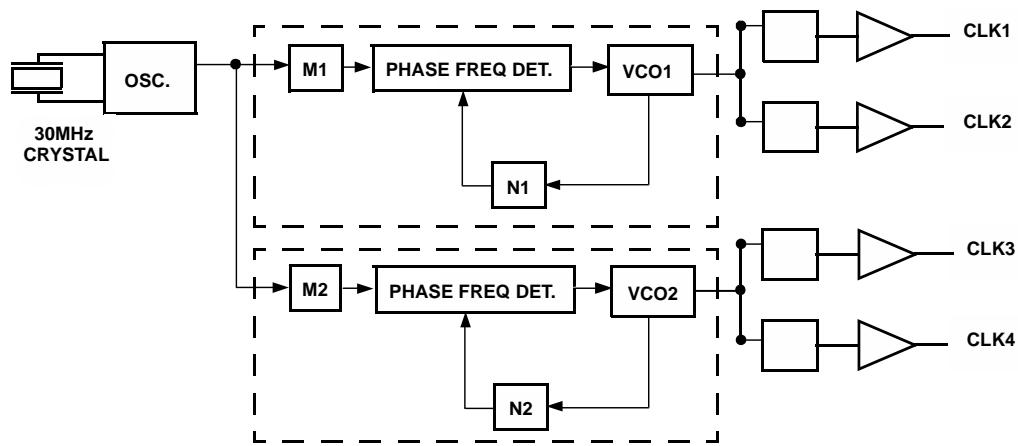
Applications

- Set-Top Boxes

Pinout

ISL14010, ISL14017
(16 LD QFN)
TOP VIEW



Functional Block Diagram**Pin Description**

16 LD QFN	SYMBOLS	PIN DESCRIPTION
1,14,16	VCC	Supply Voltage
2	X1	The X1 pin is the terminal 1 of an external 30MHz crystal. This pin is grounded for external CK input.
3	X2	The X2 pin is the terminal 2 of external 30MHz crystal, or external clock input.
4, 5, 7	GND	Ground
8	CLK1	CLK1 Output: 25MHz
10	CLK2	CLK2 Output: 30MHz
11	CLK3	CLK3 Output: 48MHz (40MHz for ISL14017)
13	CLK4	CLK4 Output: 54MHz (50MHz for ISL14017)
6, 9, 12, 15	NC	No Connect

Absolute Maximum Ratings

Voltage on VCC, CLK pins (respect to Gnd)	-0.3V to 4.0V
Voltage on X1, X2 pins (respect to Gnd)	-0.3V to 2.5V
ESD Rating	
MIL STD-883, Method 3014.	>±5kV
Machine Model.	>500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package.	58	11
Storage Temperature		-65°C to +150°C
Pb-free reflow profile		see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

DC Electrical Specifications

$V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, Typical values are at $T_A = +25^\circ\text{C}$ and $V_{CC} = 3.3V$, Unless otherwise noted

SYMBOL	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Supply Voltage	3.0	3.3	3.6	V
Supply Current	I_{CC}	Supply Current $C_L = 5\text{pF}$ on all outputs		11	15	mA
CLOCK INPUT X₂ (X₁ GROUNDED) FOR EXTERNAL CLOCK MODE						
Input High Level	V_{IH}		1.5		2.4	V
Input Level Low	V_{IL}				0.5	V
Input Current	I _{IL} , I _{IH}	V_{X2} to Ground		0.5		mA
CLOCK OUTPUTS (CLK)						
Output High Level	V_{OH}	$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$			V
		$I_{OH} = -4\text{mA}$	2.4			V
		$I_{OH} = -6\text{mA}$	2.1			V
Output Low Level	V_{OL}	$I_{OL} = 100\mu\text{A}$			0.2	V
		$I_{OL} = 4\text{mA}$			0.4	V
		$I_{OL} = 6\text{mA}$			0.75	V
Output Short Circuit Current	I_{OSC}	CLK = V_{CC} or Gnd	6	13	30	mA

AC Electrical Specifications

$C_L = 5\text{pF}$ on all outputs

SYMBOL	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Crystal Frequency	f_{IN}			30		MHz
CLOCK OUTPUTS						
Rise Time	t_R	20% to 80% V_{CC}		1.8		ns
Fall Time	t_F	80% to 20% V_{CC}		1.8		ns
Duty Cycle			40		60	%
Period Jitter	J_P	RMS		50		ps
Power Up Time	t_{PO}	$V_{CC} > 2.7\text{V}$		2		ms

Typical Performance Curves (Period Jitter)

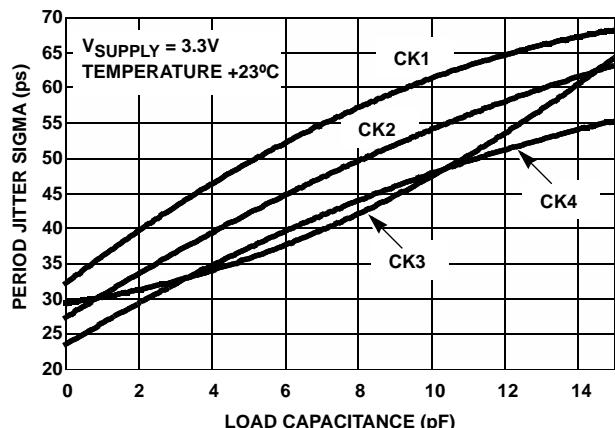


FIGURE 1. STANDARD DEVIATION vs LOAD CAPACITANCE

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

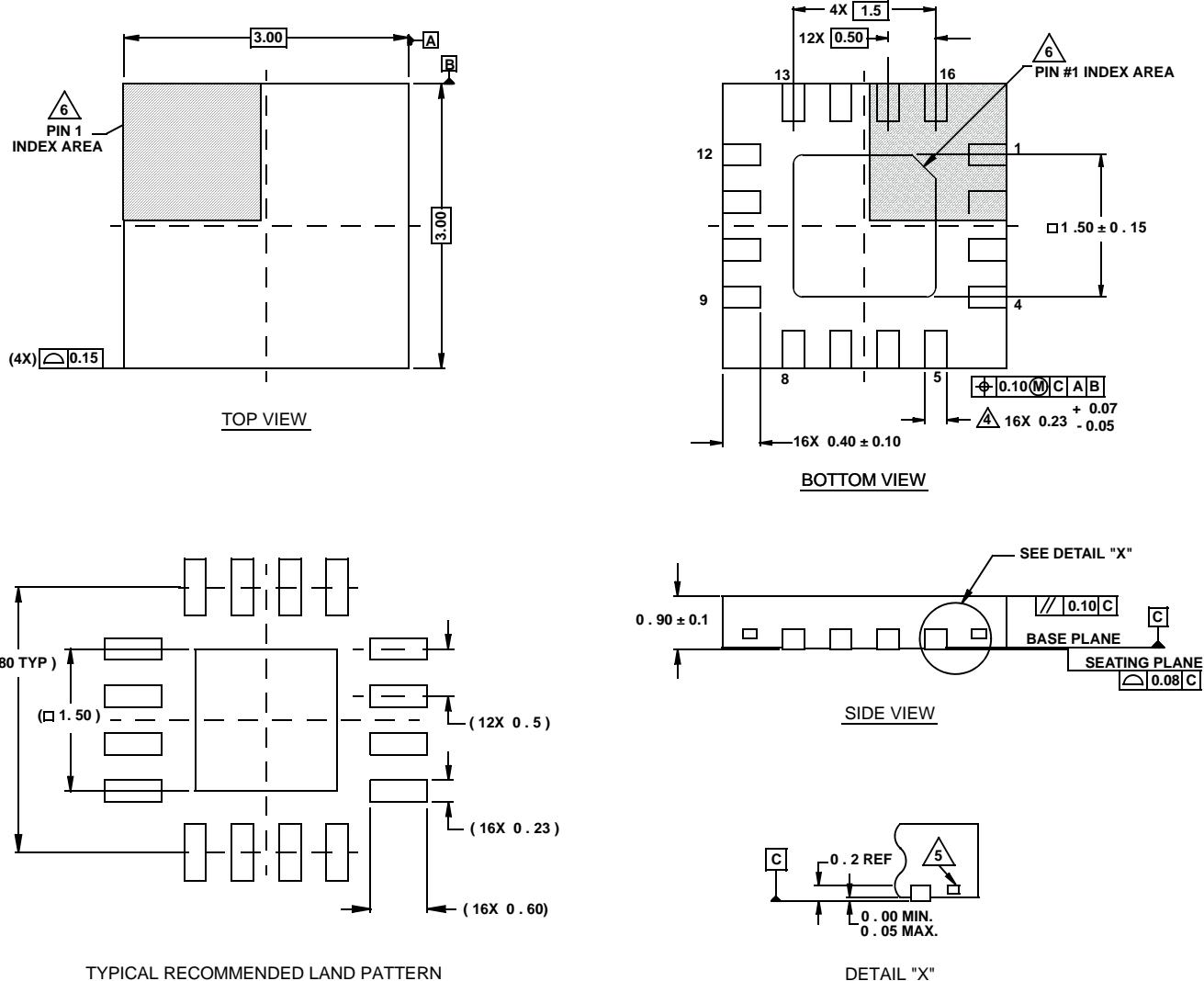
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Package Outline Drawing

L16.3x3

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 4/07



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.